ESE 330

Digital Integrated Circuits

Spring 2025

Stony Brook University
Department of Electrical and Computer Engineering

Course Description
This course presents a study of the analysis and design of digital integrated circuits. Topics include fabrication and modeling of MOS transistors; the transistor-level design of combinational and sequential digital logic; mask layout methods, design rules and processes; circuit characterization and performance estimation; computer-aided design tools and techniques. This material is directly applicable to industrial IC design and provides a strong background for more advanced courses.

Prerequisites: ESE 372

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Classes: MW 9:30am-10:50am, Frey Hall 201

Office hours: M 1:30pm-3:30pm and W 11am-1pm, or by appointment using Zoom

Teaching Assistant: Yang Xie, yang.xie.2@stonybrook.edu

Recommended Textbook:
N.H. Weste, and D. M. Harris, *"CMOS VLSI design: a circuits and systems perspective,"* Pearson, 4th edition, 2010.

Grading
1. Homework 10%
2. Midterm 30%
3. Final 40%
4. Project 20%

Project
There will be three design projects (20% of grade). The goal of the projects is the design and implementation of a modest-size CMOS digital integrated circuit. Cadence will be used as the industry-standard VLSI design and analysis tool.

Course Outline

Week 1   Introduction (ch 1.1-1.3); Diode and MOS transistor operation (ch 2.1-2.2)

Week 2   MOS transistor (C-V characteristic and non-ideal I-V effects) (ch 2.2-2.3)

Week 3   DC transfer characteristic (ch 2.5)

Week 4   IC manufacturing (ch 3.1 - 3.3), Delay: RC delay model (ch 4.1-4.3)

Week 5   Delay: Linear delay model (ch 4.4 - 4.6)

Week 6   Power (ch 5.1-5.4)

Week 7   Interconnect (ch 6.1-6.4).

Week 8   Midterm. Robustness: variability and scaling (ch 7.2 and 7.4)

Week 9   Combinational circuit design (ch 9.2)

Week 10   Combinational circuit design (ch 9.3)

Week 11   Sequential circuit design (ch 10.2)

Week 12   Sequential circuit design (ch 10.3)

Week 13   Datapath Subsystems (ch 11.2-11.4)

Week 14   Array subsystems (ch 12.2 - 12.3)

Goals:
The course is designed to provide students with in-depth analysis and design capability required for digital integrated circuits.

Objectives:
Understand the I-V characteristics of deep-submicron MOS transistors.
Understand the limited validity of simple I-V MOS models and be able to extract model parameters.
Calculate the device parasitic capacitances.
Calculate the logic high/low input/output voltages of a specified NMOS and CMOS inverter and draw the transfer curve and calculate the noise margins of a specified CMOS inverter.
Design simple NMOS and CMOS logic gates for speed, area or power.
Analyze and design static and dynamic latches and flip-flops.
Be proficient at using a circuit simulator to study the circuit response.
Understand the sources of power dissipation.
Apply approximate methods to calculate the delays of inverters.
Understand and apply transistor sizing techniques for minimizing delay through a single combinational logic gate or a chain of logic gates.
Analyze and design dynamic logic gates.
Understand the architecture of ROM and RAM circuits.
Analyze and design a memory array decoder.
Analyze and design an SRAM memory cell.
Understand and apply the Elmore delay formula for RC delay calculations.

How We Will Communicate:

This course uses Brightspace for the facilitation of communications between faculty and students, submission of assignments, and posting of grades and feedback. To log into Brightspace, go to https://brightspace.stonybrook.edu and click "Launch Brightspace" to log in with your SBU NetID. For more information and support options, visit DoIT's Brightspace service page.

You must have an active Stony Brook University email account and access to the Internet. All instructor correspondence will be sent to your SBU email account. **Plan on checking your SBU email account regularly for course-related messages.** To log in to Stony Brook Google Mail, go to http://www.stonybrook.edu/mycloud and sign in with your NetID and password.

Student Accessibility Support Center Statement

If you have a physical, psychological, medical, or learning disability that may impact your course work, please contact the Student Accessibility Support Center, Stony Brook Union Suite 107, (631) 632-6748, or at sasc@stonybrook.edu. They will determine with you what accommodations are necessary and appropriate. All information and documentation is confidential.

Academic Integrity:

Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty is required to report any suspected instances of academic dishonesty to the Academic Judiciary. Faculty in the Health Sciences Center (School of Health Technology & Management, Nursing, Social Welfare, Dental Medicine) and School of Medicine are required to follow their school-specific procedures. For more comprehensive information on academic integrity, including categories of academic dishonesty please refer to the academic judiciary website at http://www.stonybrook.edu/commcms/academic_integrity/index.html

Critical Incident Management:

Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of Student Conduct and Community Standards any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn. Faculty in the HSC Schools and the School of Medicine are required to follow their school-specific procedures. Further information about most academic matters can be found in the Undergraduate Bulletin, the Undergraduate Class Schedule, and the Faculty-Employee Handbook.