ESE 530 Computer-Aided Design

(Syllabus)

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Course Description

The course discusses modern techniques used in computer-aided design of analog and mixed-signal circuits and systems, including CAD for layout design, circuit sizing, topology generation and modeling. The lectures present research papers that have been published recently published in the most relevant CAD journals. Three projects are part of the required course work. Students are also expected to actively participate to the discussions in class.

Bulletin description

The course presents techniques for analyzing linear and nonlinear dynamic electronic circuits using the computer. Some of the topics include network graph theory, generalized tableau and hybrid analysis, companion modeling. Newton's method in n-dimensions, numerical integration, sensitivity analysis and optimization.

Prerequisite: BS in Electrical Engineering

No. credits: 3 credits

Grading: ABCF

Textbook: There is no textbook. Research papers will be discussed.

Grading: Three projects (each 30% of the grade) + 10% for participation to class discussions. The projects will involve software development in a high level programming language (C, C++, Java, Python, Matlab) and project report writing.

List of papers

(the list might change)

Layout Design

- R. Castro-Lopez, O. Guerra, E. Roca, F. Fernandez, “An Integrated Layout-Synthesis Approach for Analog ICs”, IEEE Transactions on CADICS, Vol. 27, No. 7, 2008.
- P.-H. Lin, Y.-W. Chang, S.-C. Lin, “Analog Placement based on Symmetry-Island Formulation”, IEEE Transactions on CADICS, Vol. 28, No. 6, 2009.

Transistor Sizing

- M. del Mar Hershenson, S. Boyd, T. Lee, “Optimal Design of a CMOS Op-Amp via Geometric Programming”, IEEE Transactions on CADICS, Vol. 20, No. 1, 2001.
- T. Massier, H. Graeb, and U. Schlichtmann, “The sizing rules method for CMOS and bipolar analog integrated circuit synthesis,” IEEE Transactions CADICS, Vol. 27, No. 12, pp. 2209–2222, Dec. 2008.
- F. Gong, X. Liu, H. Yu, S. Tan, J. Ren, L. He, “A Fast Non-Monte-Carlo Yield Analysis and Optimizationby Stochastic Orthogonal Polynomials”, ACM Transactions on Design Automation of Electronic Systems, Vol. 17, No. 1, 2012.
- B. Li, F. Fernandez, G. Gielen, “Efficient and accurate analog yield optimization and variation-aware circuit sizing based on computational intelligence techniques”, IEEE Transactions on CADICS, Vol. 30, No. 6, 2011.
- B. Liu, N. Deferm, D. Zhao, P. Reynaert, G. Gielen, “An Efficient High-Frequency Linear RF Amplifier Synthesis Method Based on Evolutionary Computation and Machine Learning Techniques”, IEEE Transactions on CADICS, Vol. 31, No. 7, 2012.
- G. Stehr, H. Graeb, K. Antreich, “Analog performance space exploration by normal-boundary intersection and by fourier-motzkin elimination”, IEEE Transactions on CADICS, Vol. 26, No. 10, 2007.
- B.De Smedt, G. Gielen, “WATSON: Design space boundary exploration and model generation for analog and RF IC design”, IEEE Transactions on CADICS, Vol. 22, No. 2, 2003.
- H. Tang, H. Zhang, A. Doboli, "Refinement based Synthesis of Continuous-Time Analog Filters Through Successive Domain Pruning, Plateau Search and Adaptive Sampling", IEEE Transactions CADICS, Vol. 25, No. 8, pp. 1421-1440, 2006.

Topology Synthesis

- E. Martens, G. Gielen, “Classification of analog synthesis tools based on their architecture selection mechanisms”, Integration, the VLSI Journal, Vol. 41, 2008.

- R. Harjani, R. Rutenbar, R. Carley, “OASYS: A framework for analog circuit synthesis”, IEEE Transactions CADICS, Vol. 8, no. 12, pp. 1247–1266, Dec. 1989.

- H. Y. Koh, C. H. Séquin, and P. R. Gray, “OPASYN: A compiler for CMOS operational amplifiers,” IEEE Transactions CADICS, Vol. 9, No. 2, pp. 113–125, Feb. 1990.

- T. Sripramong, C. Toumazou, “The Invention of CMOS Amplifiers using Genetic Programming and Current Flow Analysis”, IEEE Transactions on CADICS, Vol, 21, No. 11, 2002

- T. McConaghy, P. Palmers, M. Steyeart, G. Gielen, “Variation-aware Structural Synthesis of Analog Circuits via Hierarchical Building Blocks and Structural Homotopy”, IEEE Transactions on CADICS, Vol. 28, No. 9, 2009.

Modeling

- A. Doboli, R. Vemuri, "A Regularity-based Hierarchical Symbolic Analysis Method for Large-scale Analog Networks", IEEE Transactions on Circuits & Systems II, Vol. 48, No 11, pp. 1054-1067, 2001.

- Y. Wei, A. Doboli, “Structural macromodeling of analog circuits through model decoupling and transformation”, IEEE Transactions on CADICS, Vol. 27, No. 4, 2008.

- Y. Feng, A. Mantooth, “Algorithms for automatic model topology formulation”, IEEE Transactions on CADICS, Vol. 28, No. 4, 2009.

- P. Li, L. Pileggi, “Compact reduced-order modeling of weakly nonlinear analog and RF circuits”, IEEE Transactions on CADICS, Vol. 24, No. 2, 2005.

- H. Zhang, A. Doboli, "A Scalable Sigma-Space Based Methodology for Modeling Process Parameter Variations in Analog Circuits", Microelectronics Journal, Elsevier, 2009.

- M. Storace, I. Feo, “Piecewise-linear approximation of nonlinear dynamical systems”, IEEE Transactions on Circuits & Systems I, Vol. 51, No., 4, 2004.

- E. Klumperink, B. Nauta, “Systematic Comparison of HF CMOS Transconductors”, IEEE Transactions on Circuits and Systems – II, Vol. 50, No. 10, 2003.

- C. Ferent, A. Doboli, “Symbolic Matching and Constraint Generation for Systematic Comparison of Analog Circuits”, IEEE Transaction on CADICS, 2013, to appear.