ESE 545 Computer Architecture Spring 2015

Course Description: This course focuses on the techniques of quantitative analysis and evaluation of modern computer systems. The emphasis is on instruction set design, pipelining, instruction and thread level parallelism, and memory hierarchies. Students will undertake a design project on the multimedia processor design related to the course contents.

The project is to be done with a use of hardware description languages, such as VHDL or Verilog, as well as modern CAD systems, such as Cadence, Mentor Graphics, etc.

Neither VHDL/Verilog languages nor the use of CAD systems will be taught in the class. Students are strongly encouraged to begin learning these tools individually starting from the first week of the class.

Lectures: 152 Light Engineering Monday 7:00 - 9:40 PM

Instructor: Mikhail Dorojevets
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Office hours: M 9:50-11:50 AM

Text: J. Hennessy and D. Patterson, Computer Architecture: A Quantitative Approach**, Fifh edition**, Morgan Kaufmann Publishers (Elsevier), 2012, ISBN: 978-0-12-383872-8.

Other Highly Recommended Books:

1. Peter J. Ashenden. The Designer's Guide to VHDL, 3rd edition, Morgan Kaufmann Publishers, 2008, ISBN: 978-0-12-088785-9.
2. Samir Palnitkar. Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall, 2003, ISBN: 0130449113.

Exam: There will be one ("late mid-term") exam in April.
Project presentation deadline: Last week of classes.

Grading:

Exam:	50%
Project (one or two person teams):	50%

If you have a physical, psychological, medical or learning disability that may impact on your ability to carry out assigned course work, I would urge that you contact the staff in the Disabled Student Services office (DSS), room 133 Humanities, 632-6748/TDD. DSS will review your concerns and determine, with you, what accommodations are necessary and appropriate. All information and documentation of disability is confidential.